

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE  
(Rev. 2-32) PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
SP018.C3APPL. NO.  
To be assigned 08/937,361INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

(Use several sheets if necessary)

APPLICANT  
GARG et al.FILING DATE  
herewith

GROUP

2783

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA1	4	2	1	2	0	7	6	07/08/80	John P. Connors			
	AB1	5	1	2	5	0	9	2	06/92	Prener			
	AC1	5	2	0	1	0	5	6	04/93	Daniel et al.			
	AD1	5	2	4	1	6	3	6	08/93	Kohn			
	AE1	5	4	8	7	1	5	6	01/23/96	Popescu et al.			
	AF1												
	AG1												
	AH1												

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
														YES	NO
✓ ✓ ✓ ✓ ✓	AI1	0	1	7	0	2	8	4	02/05/86	Europe EP	—	—	X		
	AJ1	0	2	1	3	8	4	3	03/11/87	Europe EP	—	—	X		
	AK1	0	2	4	1	9	0	9	10/87	Europe ED	—	—	X		
	AL1	2	1	9	0	5	2	1	11/18/87	United Kingdom UK	—	—	X		
	AM1	0	4	5	4	6	3	6	10/31/91	Europe EP	—	—	X		

## OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

AN1	Patterson et al., "A VLSI RISC," <i>IEEE Computer</i> , Volume 15, No. 9, pp. 8-18, September 1982.
AO1	Maejima et al., "A 16-bit Microprocessor with Multi-Register Bank Architecture", <i>Proc. Fall Joint Computer Conference</i> , November 2-6, 1986, pp. 1014-1019.
AP1	Birman et al., "Design of a High-Speed Arithmetic Datapath," <i>IEEE</i> , pp. 214-216, 1988.
AQ1	Ruby B. Lee, "Precision Architecture," <i>IEEE Computer</i> , pp. 78-91, January 1989.
AR1	Molnar et al., "Floating-Point Processors," <i>IEEE Intl. Solid-State Circuits Conf.</i> , pp. 48-49, plus Figure 1, February 1989.
AS1	Steven et al., "Harp: A Parallel Pipelined RISC Processor," <i>Microprocessors and Microsystems</i> , Vol. 13, No. 9, pp. 579-586, November 1989.
AT1	Groves et al., "An IBM Second Generation RISC Processor Architecture", <i>35TH IEEE Computer Society International Conference</i> , February 26, 1990, pp. 166-172.
AU1	Miller et al., "Exploiting Large Register Sets", <i>Microprocessors and Microsystems</i> , Vol. 14, No. 6, July 1990, pp. 333-340.
AV1	Adams et al., "Utilising Low Level Parallelism in General Purpose Code: The HARP Project", <i>Microprocessing and Microprogramming</i> , Vol. 29, No. 3, October 1990, pp. 137-149.
AW1	Daryl Odner et al., "Architecture and Computer Enhancements for PA-RISC Workstations," <i>Proc. from IEEE Compcon</i> , San Francisco, CA, pp. 214-218, February 1991.

EXAMINER

LARRY D. DONAGHUE  
PRIMARY EXAMINER

DATE CONSIDERED

5/15/98


Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP §09; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Form PTO-1449 [6-4])

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP018.C3	APPLICATION NO. 08/937,361
	APPLICANT Garg et al.	
	FILING DATE September 25, 1997	GROUP 2783

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1						
	AB1						
	AC1						
	AD1						
	AE1						
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
	AR	1	Colin Hunter, "Series 3200 Programmer's Reference Manual," Prentice-Hall Inc., Englewood Cliffs, NJ, 1987, pp. 2-4, 2-21, 2-23, 6-14 and 6-126.
	AS	1	
	AT	1	

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	5/15/98
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